

Description

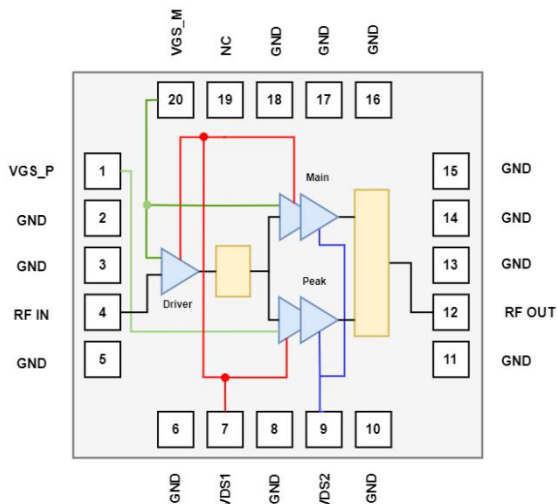
The H9G3438M15P is a LDMOS MMIC Integrated Asymmetrical Doherty Amplifier based on 3-Stage topology with 15W saturated output power covering frequency range from 3.4 - 3.8 GHz.

The amplifier is 50Ω in/out matched with a small compact footprint of 7x7 mm which makes it ideal for integration.



LGA 7x7 mm 20-Pins Plastic Package

Block Diagram



Features

- Operating Frequency Range: 3.4-3.8 GHz
- Operating Drain Voltage: +28V
- P1dB: 14W (+41.5 dBm)
- P3dB: 15.1W (+41.8 dBm)
- 50 Ω Input/Output matched
- Integrated Input Divider
- Integrated Output Combiner
- Integrated Asymmetrical Doherty Final Stage
- Average Power as Driver: 27dBm (0.5W)
- High Efficiency: 21%, 5MHz WCDMA
- High Gain: 32.5dB, 5MHz WCDMA
- Small footprint package: LGA 7x7 mm

Applications

- 3GPP 5G NR FR1 n77(n78), n48(CBRS) and 4G-LTE band B42/43/48
- Power Amplifier for Small Cells
- Driver Amplifier for Micro and Macro Base Stations
- Active Antenna Array for 5G mMIMO

Order Information

Part Number	Description
H9G3438M15P	Reel Package
H9G3438M15P-EVB	3.4-3.8 GHz EVB

Typical Performances

RF Characteristics (Pulsed CW)

Freq(MHz)	P1dB(dBm)	P3dB(dBm)	Gain(dB)*	Eff(%)*	IRL(dB)*
3400	41.5	41.8	32.9	20.9	-17.1
3600	41.6	41.9	32.2	19.0	-19.6
3800	41.4	41.8	33.0	20.0	-16.2

Test conditions, unless otherwise noted: 25 °C, 10% Pulse, Vds = +28V, Idq_M= 34mA, VGS_P=VGS_M-0.47V, Test on Watech Application Board.

*Pout=27dBm

RF Characteristics (WCDMA)

Freq(MHz)	Gain (dB)	Eff(%)	ACPR_5MHz(dBc)*	ACPR_10MHz(dBc)*
3400	33.0	21.4	-34.2	-52.0
3600	32.3	19.2	-36.3	-53.4
3800	33.0	20.6	-34.0	-51.7

Test conditions, unless otherwise noted: 25 °C, Vds = +28V, Idq_M= 34mA, VGS_P=VGS_M-0.47V, Pave = 27 dBm, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF, test on WATECH Application Board.

*Uncorrected DPD

Absolute Maximum Ratings

Parameter	Range/Value	Units
Drain voltage (VDSS)	-0.5 to 65	V
Gate voltage (VGS)	-5 to 10	V
Storage Temperature (TSTG)	-55 to 150	°C
Case Temperature (TC)	-40 to 125	°C
Junction Temperature (TJ)	-40 to 175	°C

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage V(BR)DSS	Vgs=0V, Ids=15.8uA	65	-	80	V
Gate-Source Threshold Voltage VGS(th)	Vds=10V, Ids=15.8uA	1.2	-	2.0	V
Drain Leakage Current IDSS	Vgs=0V, Vds=28V	-0.1	-	1.5	uA
Gate Leakage Current IGSS	Vgs=10V, Vds=0V	-0.1	-	0.5	uA

Test conditions unless otherwise noted: 25 °C

RF Characteristics (Pulsed CW)

Parameter	Conditions	Min	Typ	Max	Unit
P1dB	Freq=3.4GHz	40.0	41.5	-	dBm
P3dB	Freq=3.4GHz	40.8	41.8	-	dBm
IRL	Freq=3.4GHz, Pout=27dBm	-	-15.0	-8.0	dB
P1dB	Freq=3.8GHz	40.0	41.4	-	dBm
P3dB	Freq=3.8GHz	40.7	41.7	-	dBm
IRL	Freq=3.8GHz, Pout=27dBm	-	-15.0	-8.0	dB

Test conditions unless otherwise noted: 25°C, 10% Pulse, Vds = 28 V, Idq_M = 34 mA, VGS_P = VGS_M - 0.47V, test on WATECH Production Board.

RF Characteristics (WCDMA)

Parameter	Conditions	Min	Typ.	Max	Unit
Gain	Freq=3.4GHz, Pout=27dBm	29.5	32.5	-	dB
Eff	Freq=3.4GHz, Pout=27dBm	18.5	22.0	-	%
ACPR@5MHz	Freq=3.4GHz, Pout=27dBm	-	-34.0	-30.0	dBc
Gain	Freq=3.8GHz, Pout=27dBm	29.5	32.5	-	dB
Eff	Freq=3.8GHz, Pout=27dBm	16.5	20.0	-	%
ACPR@5MHz	Freq=3.8GHz, Pout=27dBm	-	-34.0	-30.0	dBc

Test conditions unless otherwise noted: 25°C, Vds = 28 V, Idq_M = 34 mA, VGS_P = VGS_M - 0.47V, Pavg = 27 dBm, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on WATECH Production Board.

*Uncorrected DPD

Load Mismatch Test

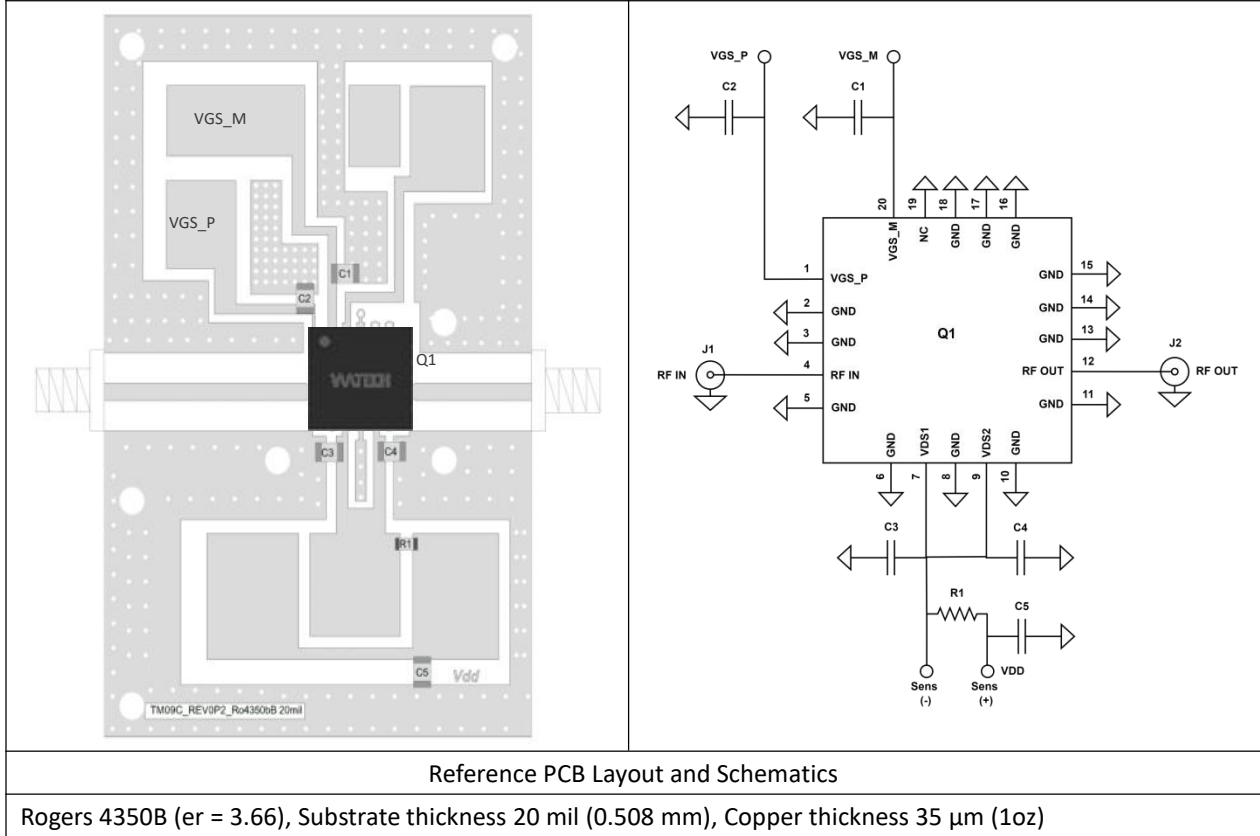
Condition	Test Result
VSWR=10:1, at all Phase Angles, V _{ds} =+28V, Id _{q_M} = 34 mA, VGS _{_P} =VGS _{_M} -0.47V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF, Frequency tested 3.4, 3.6 and 3.8 GHz P _{ave} = 27 dBm test on WATECH Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R _{th})	T _{CASE} = 90°C, 1C-WCDMA 5MHz Signal, 9.9dB PAR, P _{ave} = 27dBm	8.9	°C /W

* $R_{th} = (T_j - T_{case}) / P_{diss}$

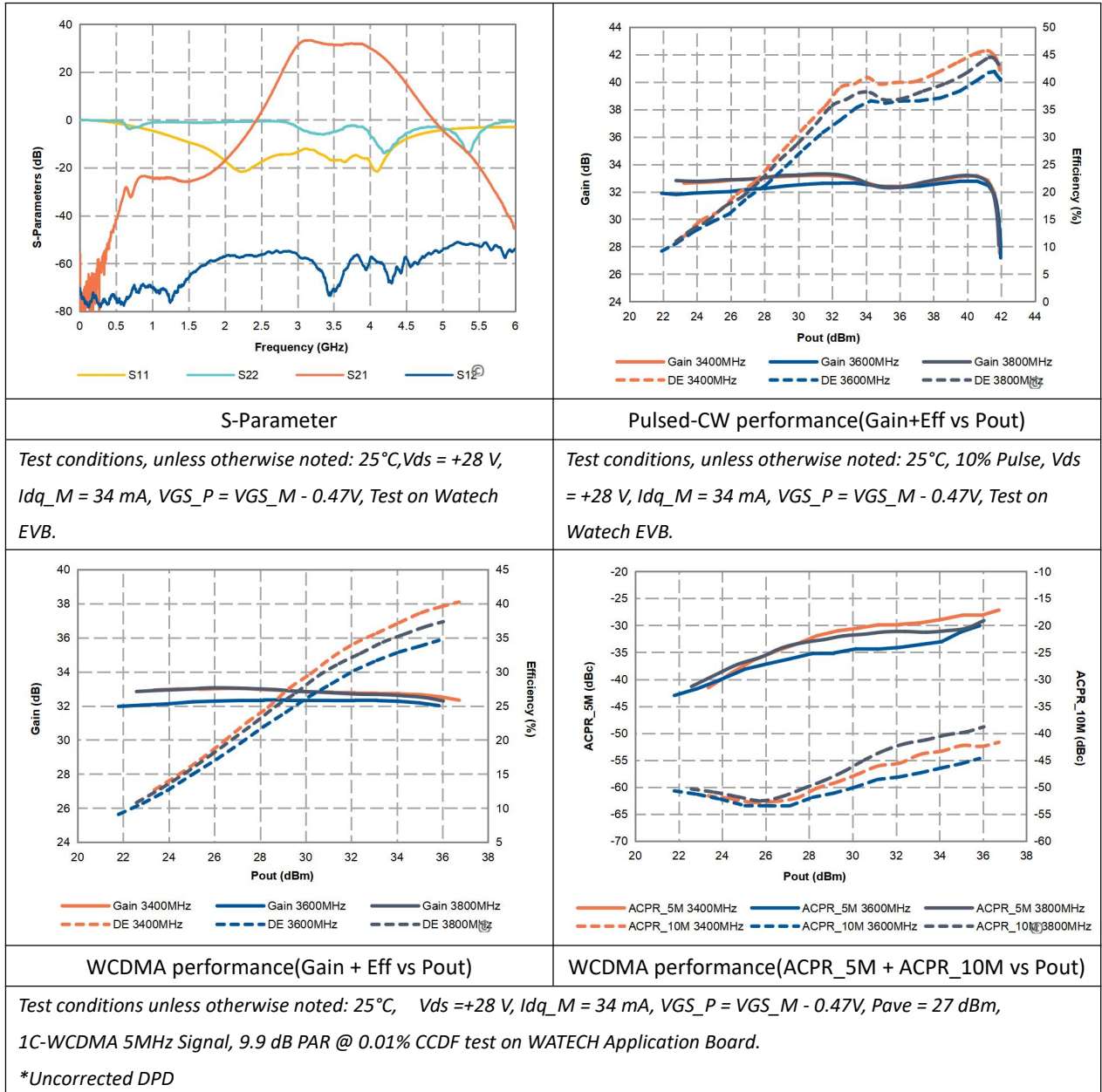
H9G3438M15P 3.4-3.8 GHz Reference Design



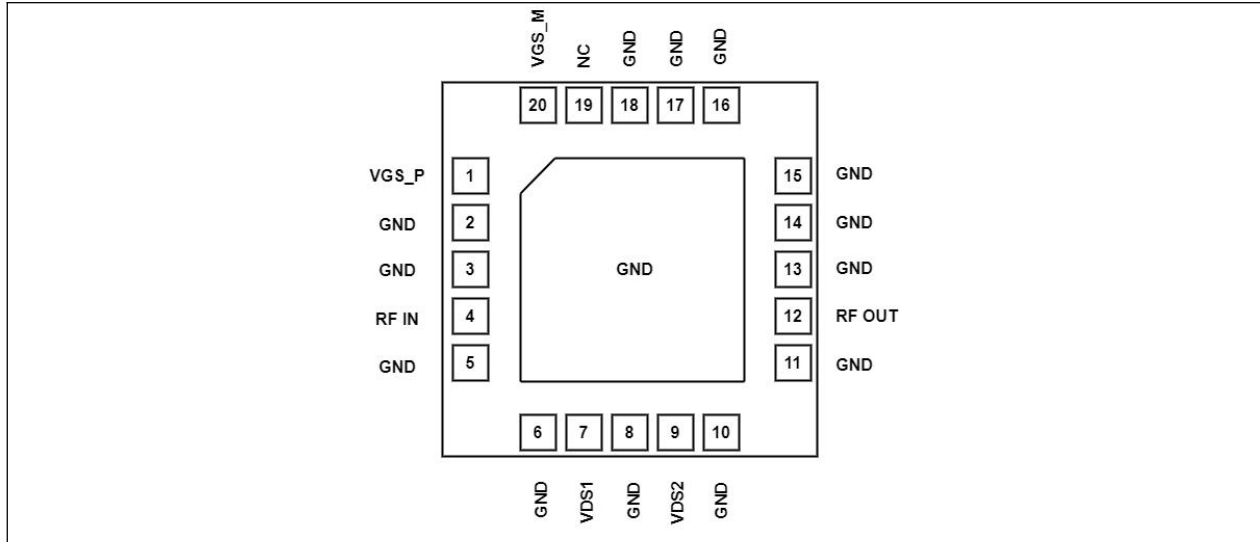
Bill of Materials (BoM) - H9G3438M15P 3.4-3.8 GHz Reference Design

Component	Type	Value	Description	P/N
Q1	Transistor	-	Transistor	H9G3438M15P
C1,C2,C3,C4,C5	Capacitor	1uF	0805, 100V	GRM21BC72A105KE01L
R1	Resistor	0.1ohm	0.5W 0.1ohms 0.5%	WSLP0805R1000DEA

Performance Plots



Pin Configuration and Description



Pin Configuration

Pin Number	Label	Description
1	VGS_P	Gate-Source Voltage Peak
2	GND	Ground
3	GND	Ground
4	RF IN	RF Input
5	GND	Ground
6	GND	Ground
7	VDS1	Drain-Source Voltage Driver
8	GND	Ground
9	VDS2	Drain-Source Voltage Final Stage
10	GND	Ground
11	GND	Ground
12	RF OUT	RF Output
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	NC	Not Connected
20	VGS_M	Gate-Source Voltage Main

Package Marking and Dimensions

marking sample

↓

Line1: fixed : device name in W/O, example:H9G3438M15P

Line2 :unfixed : Marking Lot No in W/O (Sample:E596-20140001)

Line3 :unfixed : Date Codet+"leave two blank spaces"+SS (SS : the last two digits of sub lot)

●This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Watech Product Printing Specification".

Marking

TOP VIEW

BOTTOM VIEW

SIDE VIEW

Package :	Symbol	Dimensions in mm			Dimensions in inch		
		MIN	NOM	MAX	MIN	NOM	MAX
Package :	SIPLGA						
Body Size :	X	E	6.900	7.000	7.100	0.272	0.276
	Y	D	6.900	7.000	7.100	0.272	0.276
Land Array Terminal Pad Pitch :	X	eE	1.030	---	---	0.041	---
	Y	eD	1.030	---	---	---	---
Total Thickness :	A	0.880	0.980	1.080	0.035	0.039	0.043
Mold Thickness :	Ref. M	---	0.800	---	---	0.031	---
Substrate Thickness :	c	0.150	0.180	0.210	0.006	0.007	0.008
Exposed Metal :	X	E1	4.800	4.900	5.000	0.189	0.193
	Y	D1	4.800	4.900	5.000	0.189	0.193
Exposed Metal Chamfer :	X	H	---	0.286	---	0.011	---
	Y	H1	---	0.286	---	0.011	---
LGA Array Terminal Pad Size :	X	b	0.450	0.500	0.550	0.018	0.020
	Y	L	0.370	0.420	0.470	0.015	0.017
Exposed Metal To Package Edge :	L1	0.025	0.100	0.175	0.001	0.004	0.007
	L2	0.975	1.050	1.125	0.038	0.041	0.044
	L3	0.975	1.050	1.125	0.038	0.041	0.044
Package Edge Tolerance :	aaa	0.150		0.006			
Terminal Pad Offset (Land Pad) :	bbb	0.150		0.006			
Mold Flatness :	ccc	0.100		0.001			
Terminal Pad Offset (Package) :	ddd	0.080		0.003			
Exposed Metal Offset :	eee	0.150		0.006			
LGA Array Terminal Pad Count :	n	20					

Package Dimensions


Packing Information

Package Type	Reel Size(inch)	Qty/Reel(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
LGA 7*7	13	3000	3000	15000

Tape & Reel Packaging Descriptions

Handling Precautions

Parameter	Grade	
Moisture Sensitivity Level MSL	3	
Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Charged Device Model (CDM)	Class III	JESD22-C101



RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-diffused metal-oxide semiconductor
GaN	Gallium Nitride
CW	Continuous Waveform
VSWR	Voltage Standing Wave Ratio



Revision History

Document ID	Datasheet status	Release date	Version revision record
Rev 0.1	Preliminary	2024/7/9	Preliminary datasheet
Rev 0.2	Preliminary	2024/7/15	Update mark of IC
Rev 0.3	Preliminary	2024/8/03	Update performance data and format
Rev 0.4	Preliminary	2024/8/05	Update content format
Rev 0.5	Preliminary	2024/10/22	Update reference PCB layout and schematics
Rev 0.6	Preliminary	2024/12/09	Update RF Characteristics and DC Characteristics
Rev 1.0	Product	2025/03/04	Update product related data



Contact Information

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