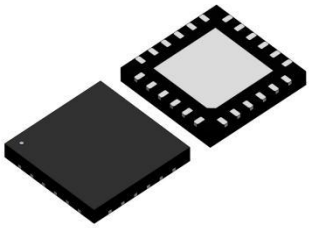
H9G2324M10Q
10W, 2.3-2.4 GHz Doherty Amplifier

Product Datasheet

Description

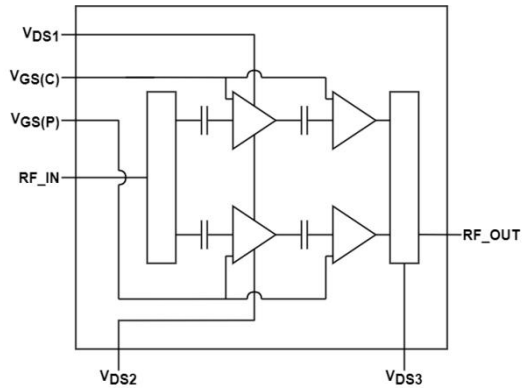
The H9G2324M10Q is a LDMOS integrated Asymmetrical Doherty 2-stage Power Amplifier designed for cellular base station applications with 1.26 W average output power covering frequency range from 2.3 to 2.4 GHz.



24 Lead QFN 6x6 mm Plastic Package

RoHS compliant

Block Diagram



Features

- Operating Frequency Range: 2.3 to 2.4 GHz
- Operating Drain Voltage: +28 V
- Saturation Output Power: 10 W
- Integrated Input Divider
- High Efficiency
- High Gain over the Frequency Range
- Small footprint package, 6mm x 6mm QFN

Applications

- 3GPP 5G NR FR1 n40 and 4G/LTE band B40.
- Power Amplifier for Small cells.
- Driver Amplifier for micro and macro base stations.
- Active antenna array for 5G mMIMO.
- Repeaters/DAS.

Order Information

Part Number	Description
H9G2324M10Q	Reel Package
H9G2324M10QEVB	2.3 - 2.4GHz EVB

Typical Performances

Freq(MHz)	P3dB(dBm)	Gain(dB)	Eff(%)	IRL(dB)
2300	40.9	27.6	48.3	-11.2
2350	41.0	27.7	48.7	-11.8
2400	41.0	27.4	47.4	-12.3

V_{DD}=28Vdc, I_{DQ}=27mA, Vgsp=Vgsm-0.6V, Pout=31 dBm, Pulsed CW, 100 us, Duty Cycle = 10%, Test on Watech EVB.

Freq(MHz)	Gain(dB)	Eff(%)	ACPR_5MHz(dBc)	ACPR_10MHz(dBc)
2300	26.5	43.5	-26.2	-39.6
2350	26.6	44.2	-26.3	-40.1
2400	26.4	43.3	-27.7	-40.5

V_{DD}=28Vdc, I_{DQ}=27mA, Vgsp=Vgsm-0.6V, Pout=31 dBm, 5MHz WCDMA, PAR=9.9 dB, Test on Watech EVB.

Absolute Maximum Ratings

Parameter	Range/Value	Units
Drain voltage (VDSS)	-0.5 to 65	V
Gate voltage (VGS)	-6 to 10	V
Storage Temperature (TSTG)	-55 to 150	℃
Case Temperature (TC)	-40 to 125	℃
Junction Temperature (TJ)	-40 to 175	℃

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
IGSS_C Gate leakage Current for Carrier	Vgs=10V, Vds=0V	/	/	1.05	uA
IGSS_P Gate leakage Current for Peak	Vgs=10V, Vds=0V	/	/	1.05	uA
IDSS Drain leakage Current	Vgs=0V, Vds=28V	/	/	2	uA
BVDS Breakdown Voltage	Vgs=0V，Ids=12.02 uA	65	/	/	V
VGS(th)_C Gate-Source threshold Voltage of Carrier	Vgs=Vds，Ids=2.5 uA	1.2	/	2	V
VGS(th)_P Gate-Source threshold Voltage of Peak	Vgs=Vds，Ids=9.52 uA	1.2	/	2	V

RF Characteristics (Pulsed CW)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	Pout=31 dBm	2.3	/	2.4	GHz
P3dB	Freq=2.4GHz	39.5	41.0	41.5	dBm

Test conditions, unless otherwise noted: 25 °C, VDD=+28Vdc, IDQ = 27 mA, Vgsp=Vgsm-0.57V, Pulse Width = 100 us, Duty Cycle = 10%,Based on FT board

RF Characteristics (WCDMA)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	Pout=31 dBm	2.3	/	2.4	GHz
Gain	Freq=2.4GHz, Pout=31dBm	25.0	26.5	28	dB
Eff	Freq=2.4GHz, Pout=31dBm	40.5	43.5	/	%
ACLR@5MHz	Freq=2.4GHz, Pout=31dBm	/	-28.0	-24.0	dBc

Test conditions, unless otherwise noted: 25 °C, VDD=+28Vdc, IDQ = 27 mA, Vgsp=Vgsm-0.57V, single-carrier, 5MHz WCDMA signal with 9.9 dB PAR @ 0.01% CCDF Based on FT board

RF Characteristics (Small-Signal)

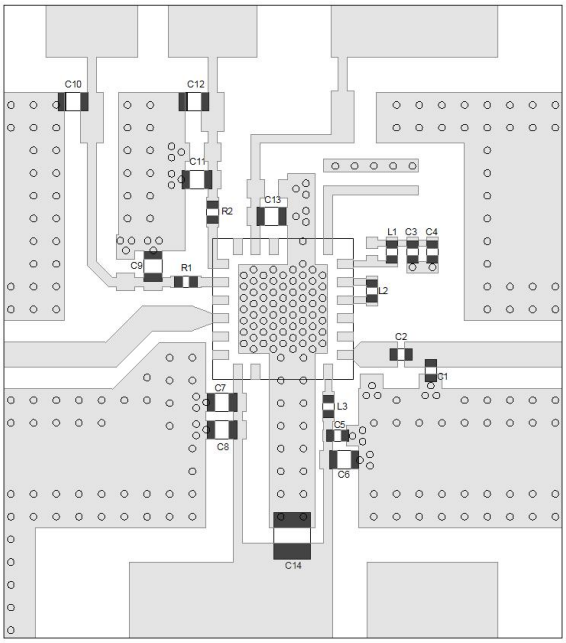
Parameter	Conditions	Min	Typ	Max	Units
Input Return Loss	Freq=2.4GHz	/	/	-8	dB

Test conditions, unless otherwise noted: 25 °C, VDD=+28Vdc, IDQ = 27 mA, Vgsp=Vgsm-0.57V, CW, Based on FT board

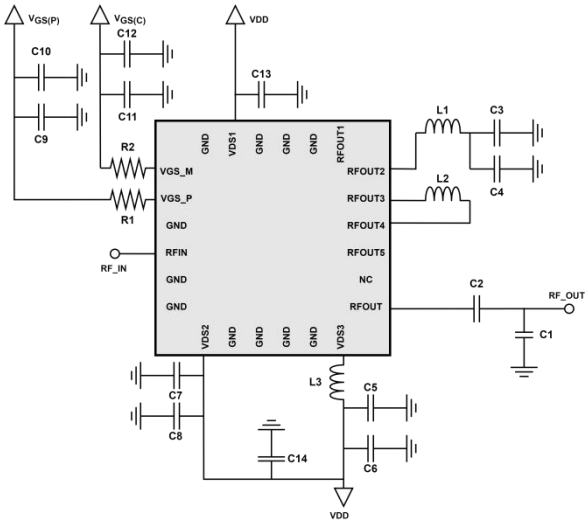
Thermal Information

Parameter	Condition	Value (Typ)	Units
Thermal Resistance Junction to Case (RTH)	T_{case}= 90℃, WCDMA single-carrier, P_{avg} = 31 dBm	8.1	C/W

H9G2324M10Q 2.3-2.4 GHz Reference Design



Reference PCB Layout



Reference Schematic

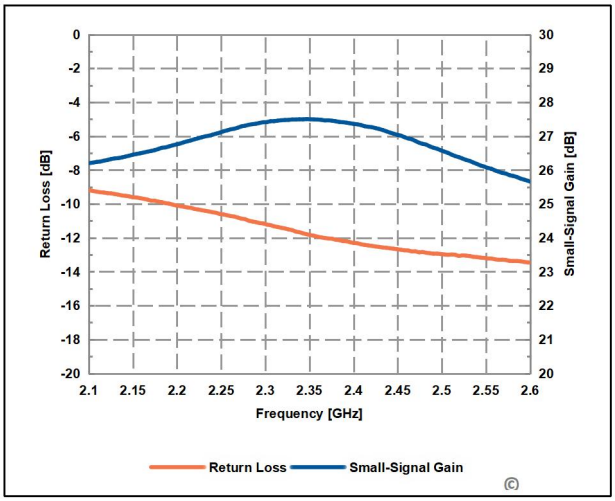
Rogers 4350B, thickness=20mil

PCB is soldered on a 25 mm by 28 mm copper base plate with 10 mm thickness

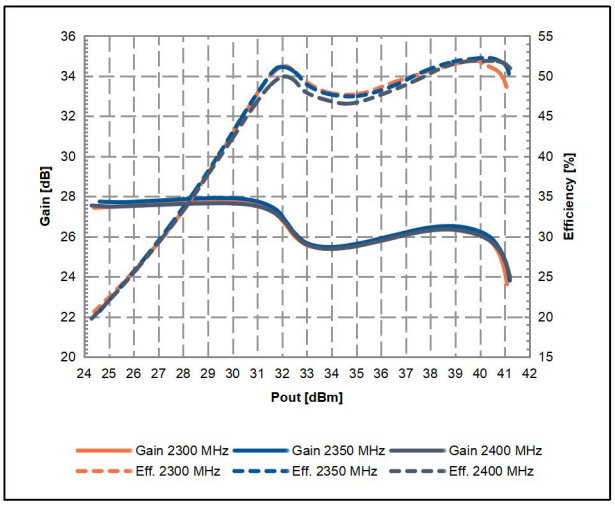
BOM-H9G2324M10Q 2.3 – 2.4 GHz Reference Design

Component	Type	Value	Description	P/N
C1	Capacitor	0.8pF	Multi-layer ceramic capacitor	GQM1555C2D0R8BB01D
C2	Capacitor	6.2pF	Multi-layer ceramic capacitor	GQM1555C2D6R2BB01D
C3	Capacitor	9.0pF	Multi-layer ceramic capacitor	GQM1555C2D9R0BB01D
C4	Capacitor	100nF	Multi-layer ceramic capacitor	GRM155B31E104KE14
C5	Capacitor	30pF	Multi-layer ceramic capacitor	GQM1555C2D300GB01D
C6 - C13	Capacitor	1 uF	Multi-layer ceramic capacitor	GRM21BC72A105KE01L
C14	Capacitor	10 uF	Multi-layer ceramic capacitor	GRM32EC72A106KE05L
L1	Inductor	5.2nH	HQ inductor	LQW15AN5N2B80D
L2	Inductor	5.4nH	HQ inductor	LQW15AN5N4B80D
L3	Inductor	8.2nH	HQ inductor	LQW15AN8N2B80D
R1, R2	Resistor	0ohm	Resistor	RC0402FR-070RL

Performance Plots

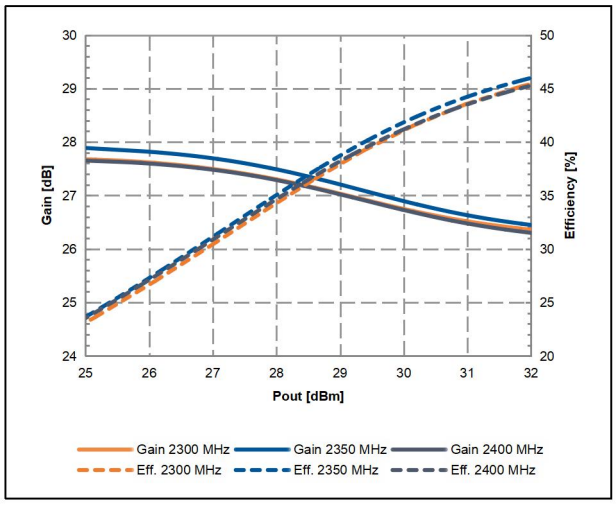


S-Parameter

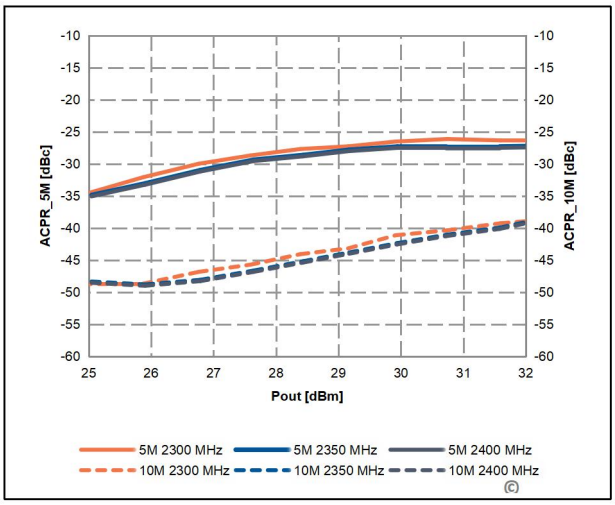


Pulsed-CW performance(Gain+Eff vs Pout)

Test conditions, unless otherwise noted: 25 °C, VDD=28 Vdc, IDQ = 27 mA, Vgsp=Vgsm-0.6V, Pulse Width = 100 us, Duty Cycle = 10%, test on WATECH EVB.



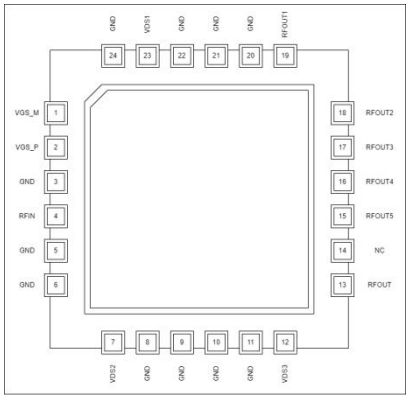
WCDMA performance(Gain+Eff vs Pout)



WCDMA performance(ACPR_5M+ACPR_10M vs Pout)

Test conditions, unless otherwise noted: 25 °C, VDD=+28Vdc, IDQ = 27 mA, Vgsp=Vgsm-0.6V, 1-carrier WCDMA, PAR=9.9 dB, test on WATECH EVB

Pin Configuration and Description



Pin Configuration

Pin Number	Label	Description
1	VGS_M	Gate-source voltage of main
2	VGS_P	Gate-source voltage of peak
3	GND	Ground
4	RFin	RF input
5	GND	Ground
6	GND	Ground
7	VDS2	Drain-source voltage of peak driver
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	VDS3	Drain-source voltage of final stage
13	RFout	RF output
14	NC	NOT CONNECTED
15	RFout5	RF output5
16	RFout4	RF output4
17	RFout3	RF output3
18	RFout2	RF output2
19	RFout1	RF output1
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	VDS1	Drain-source voltage of main driver
24	GND	Ground

Package Marking and Dimensions

Marking Spec No.	H9G2324M10Q Marking spec_A

Marking Spec

marking sample ↓

Line1: fixed : Device name

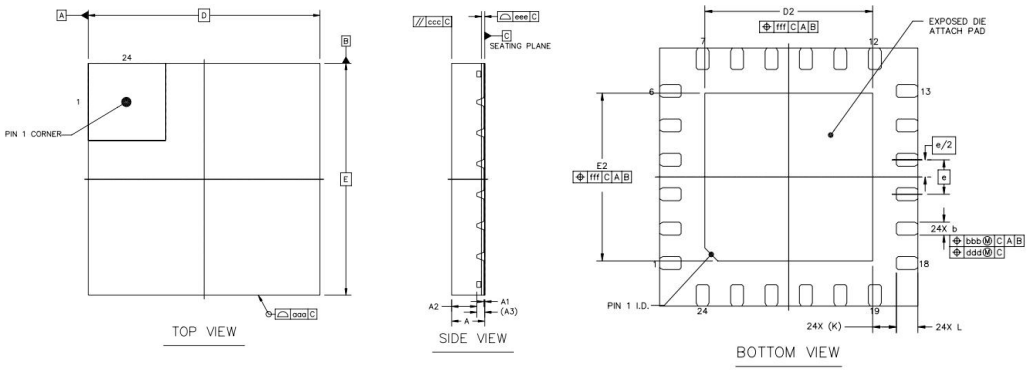
Line2 :unfixed: The last eight digits of Marking Lot No (Sample:EEYY0001)

Line3 :unfixed: Date Code+ JY

2D Code: Line2+Sub Lot No+Strip No+XXYY(Coordinates on Strip)

●This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Watech Product Printing Specification".

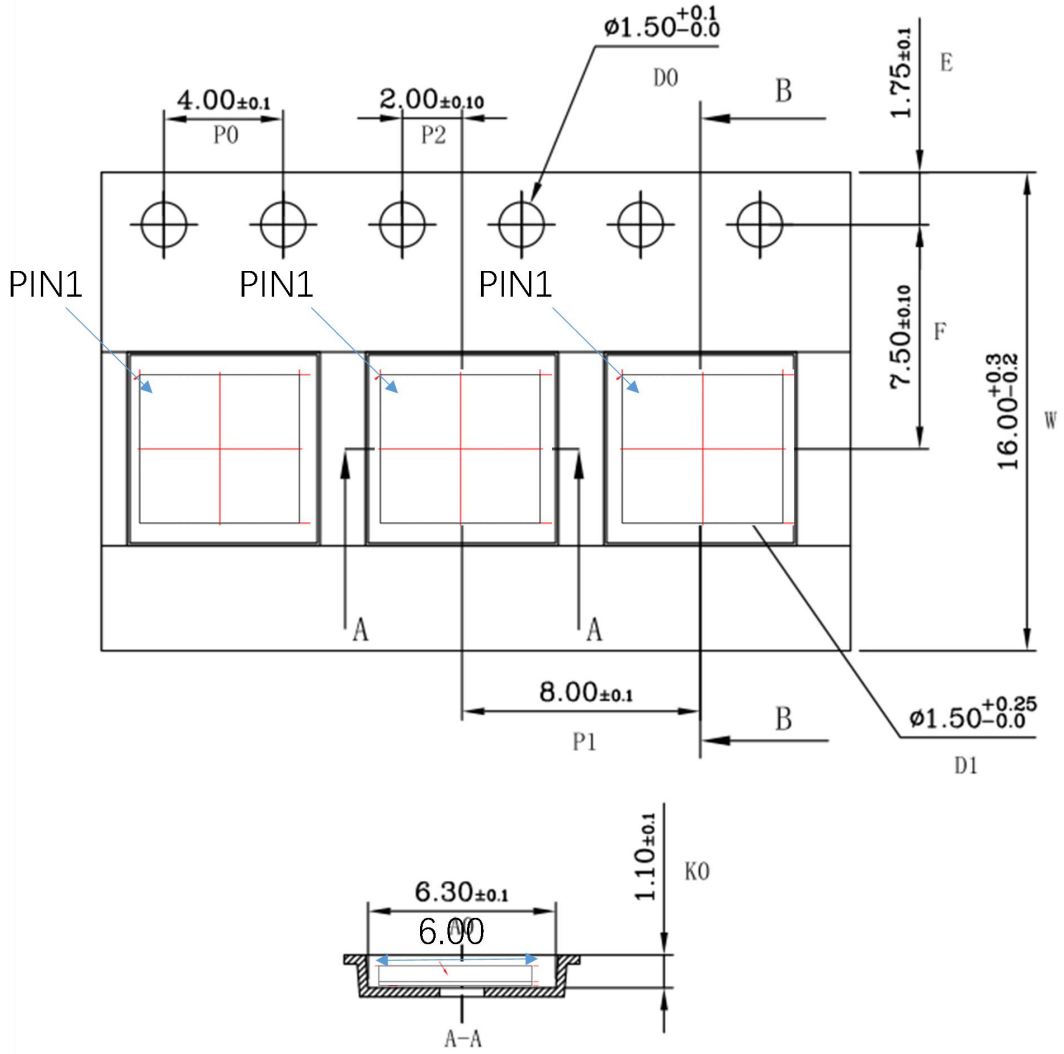
Marking



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.8 BSC	
EP SIZE	X	D2	3.8	3.9	4
	Y	E2	3.8	3.9	4
LEAD LENGTH		L	0.4	0.5	0.6
LEAD TIP TO EXPOSED PAD EDGE		K		0.55 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	

Packing Information

Package Type	Reel Size(inch)	Qty/Reel(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
QFN 6X6X0.85 24	13	3000	3000	15000



Handling Precautions

Parameter	Rating	Standard	
ESD – Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC Standard JS-001	
ESD – Charged Device Model (CDM)	C1	ANSI/ESDA/JEDEC Standard JS-002	
MSL – 260°C Convection Reflow	MSL3	IPC/JEDEC Standard J-STD-020	

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective datasheet	Design simulation	Product objective specification
Preliminary datasheet	Customer sample	Engineering samples and first test results
Product datasheet	Mass production	Final product specification

Revision history

Document ID	Datasheet status	Release date	Version revision record
H9G2324M10Q	Preliminary	2023/03	Preliminary Version
H9G2324M10Q	Product	2023/07	Product Version

Abbreviations

Acronym	Definition
LDMOS	Laterally-diffused metal-oxide semiconductor
GaN	Gallium Nitride
CW	Continuous Waveform
VSWR	Voltage Standing Wave Ratio

Contact Information

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